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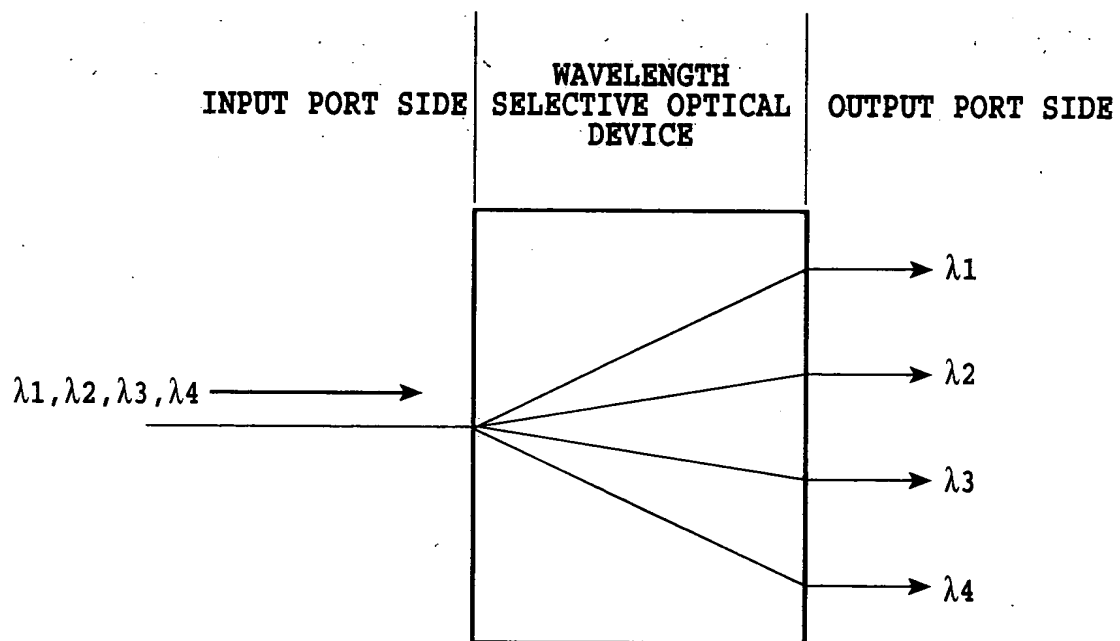


FIG.1
PRIOR ART

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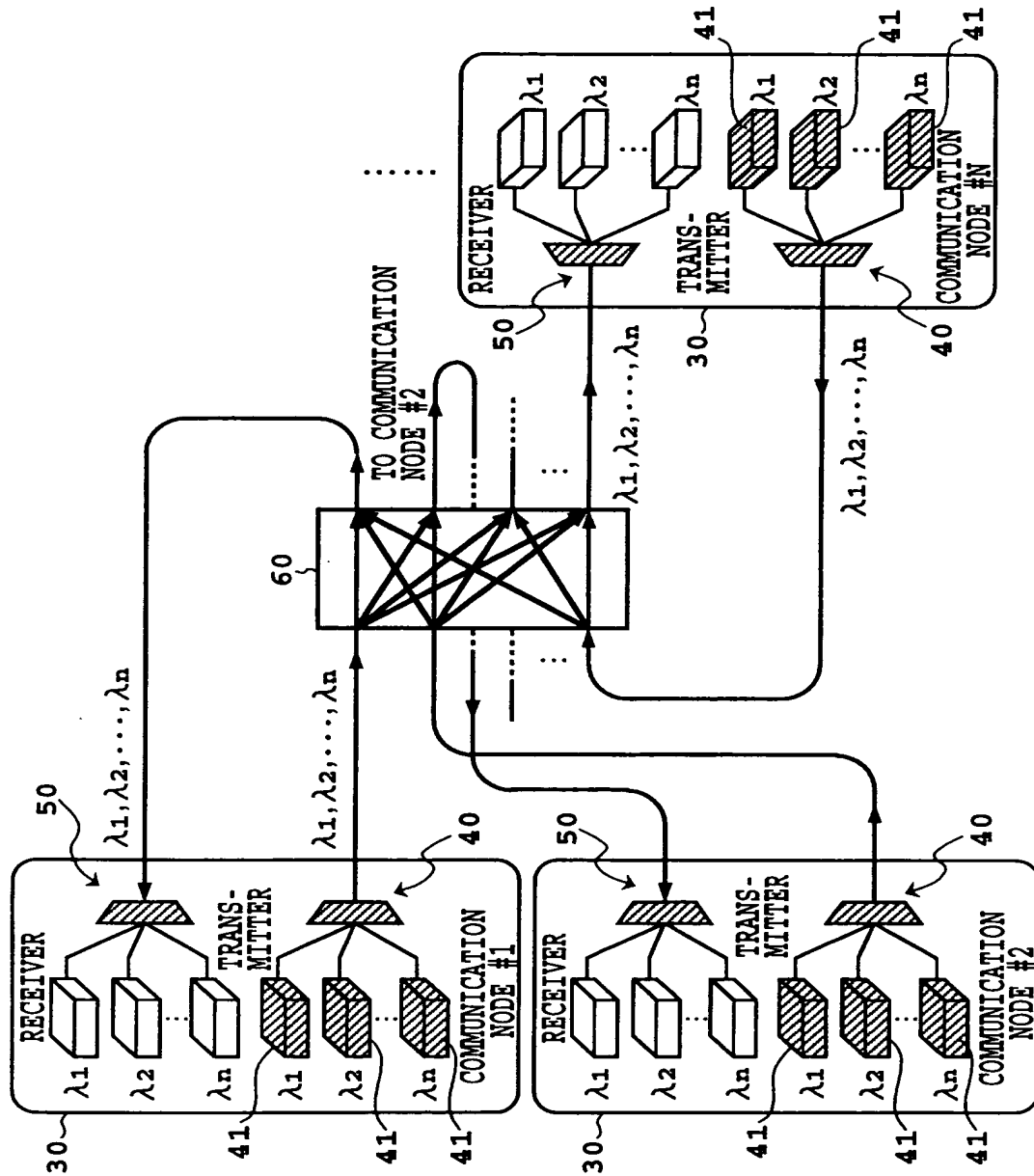


FIG.2
PRIOR ART

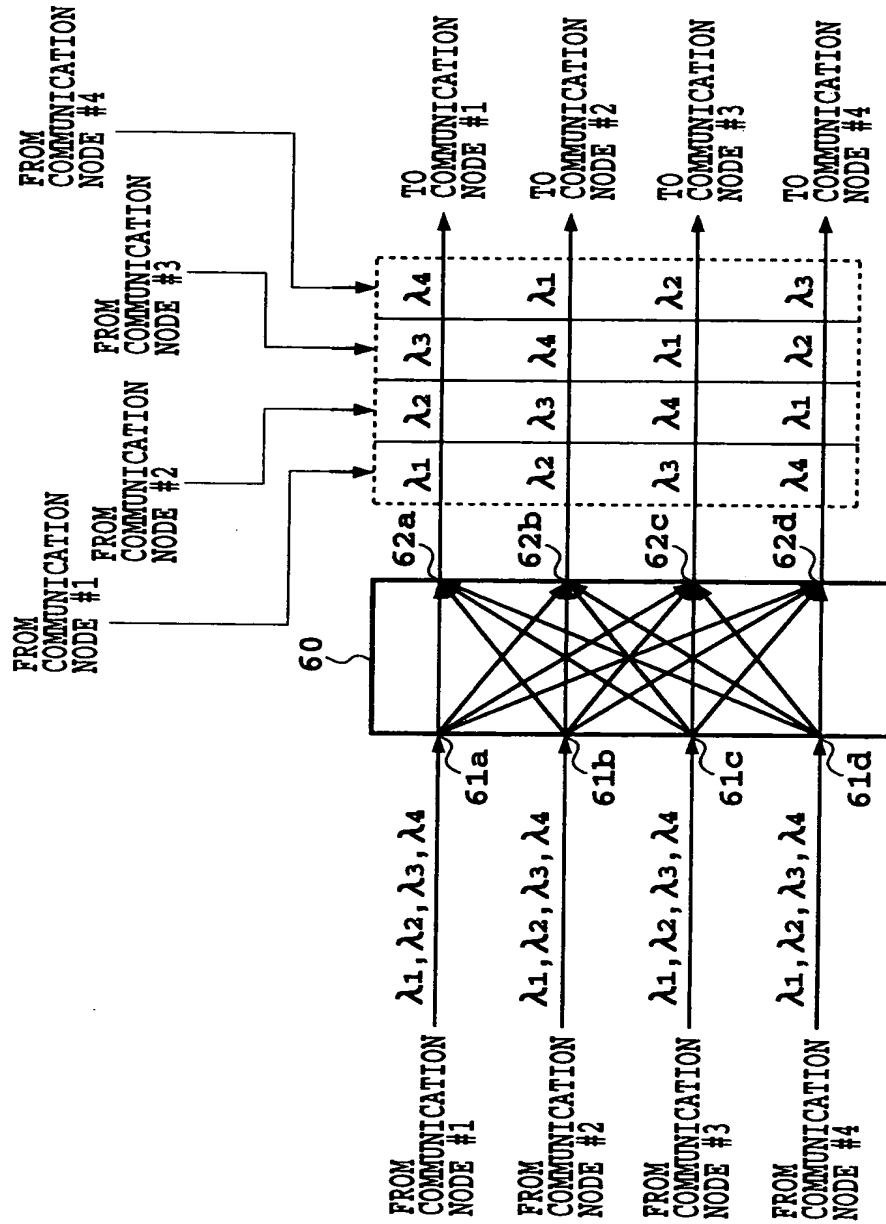


FIG. 3
 PRIOR ART

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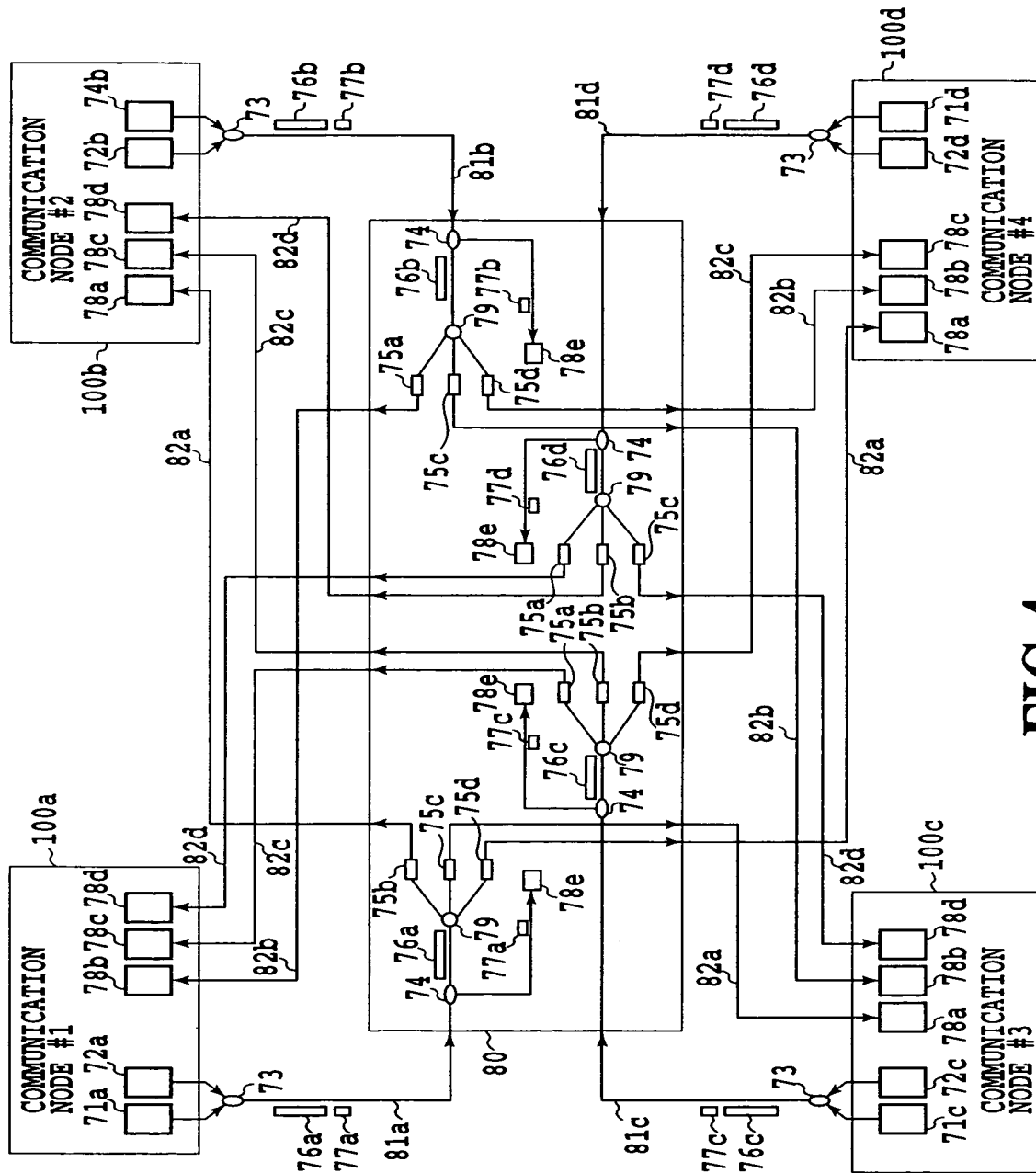


FIG. 4
PRIOR ART

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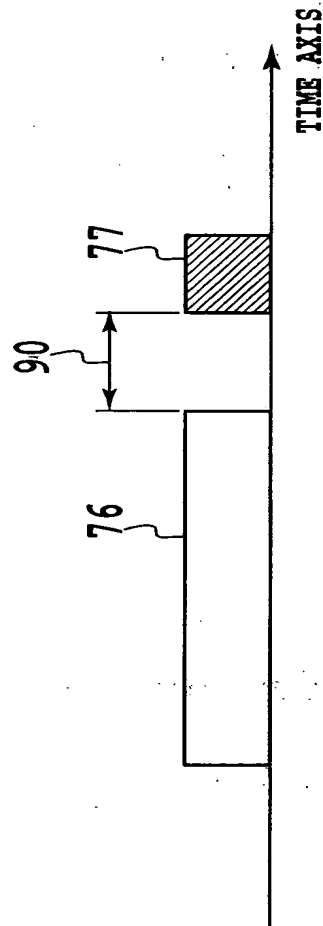


FIG.5
PRIOR ART

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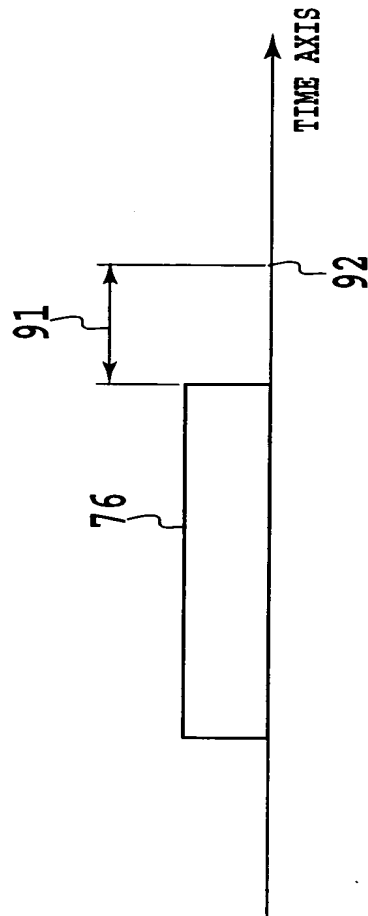


FIG.6
PRIOR ART

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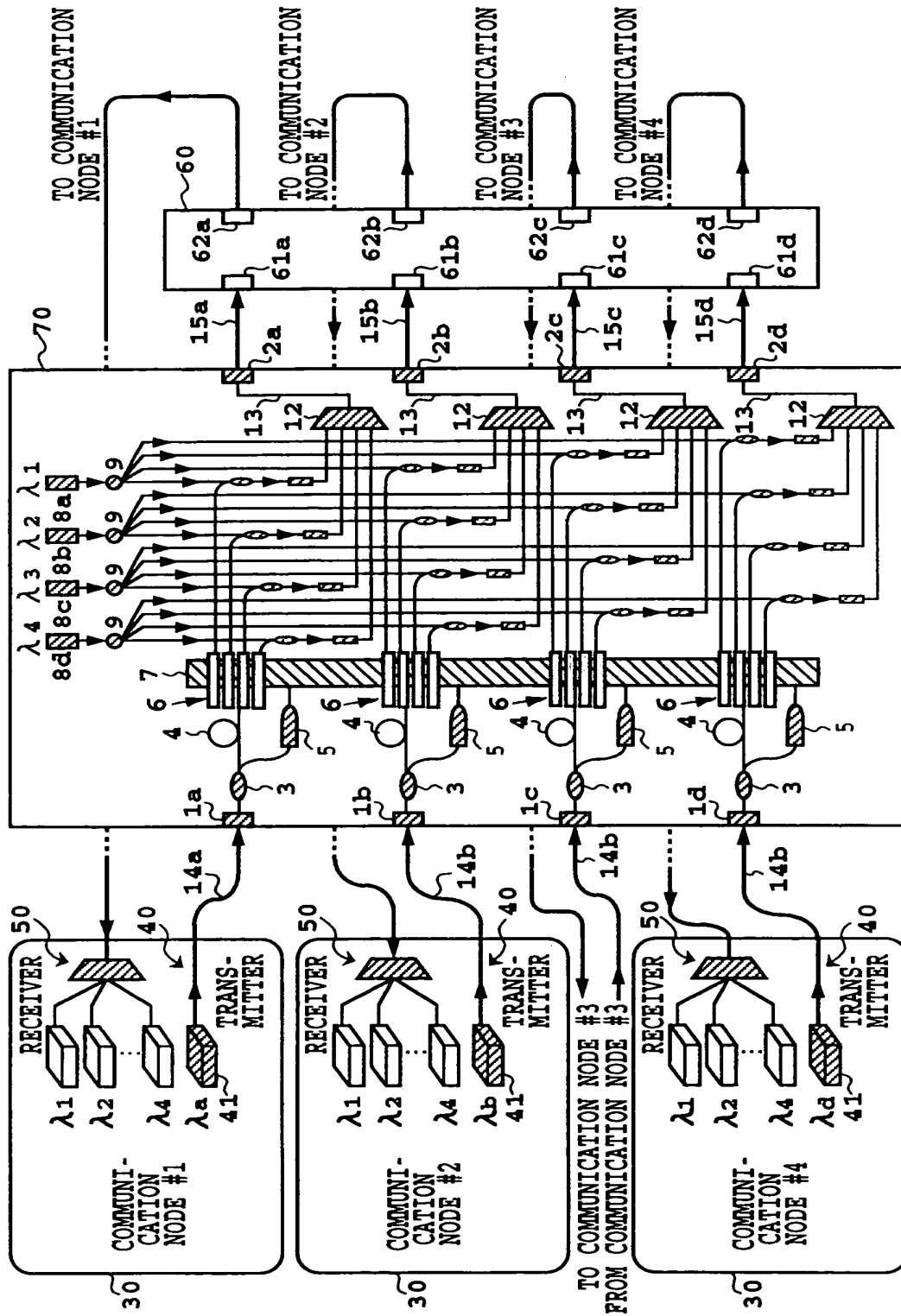


FIG. 7

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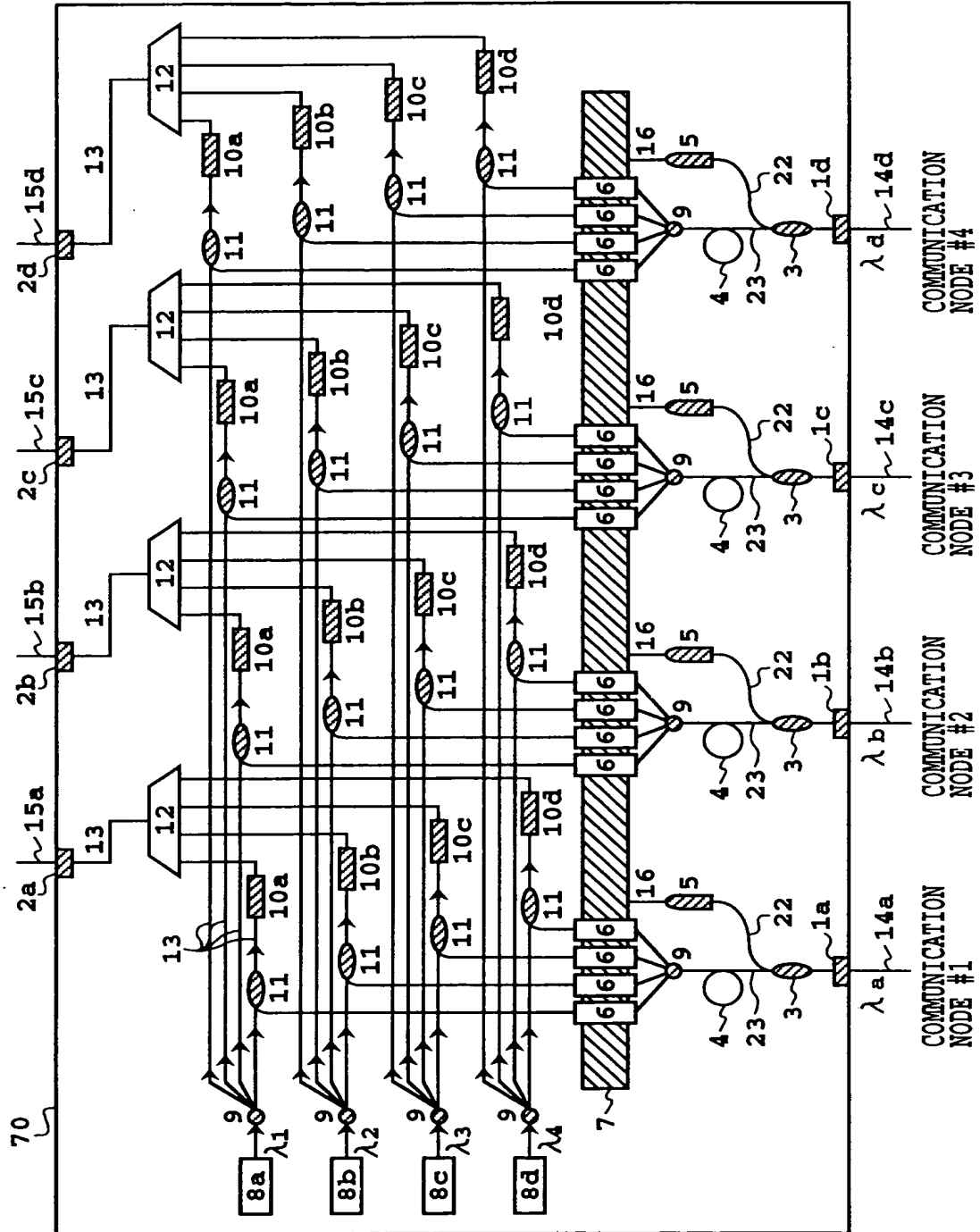


FIG.8

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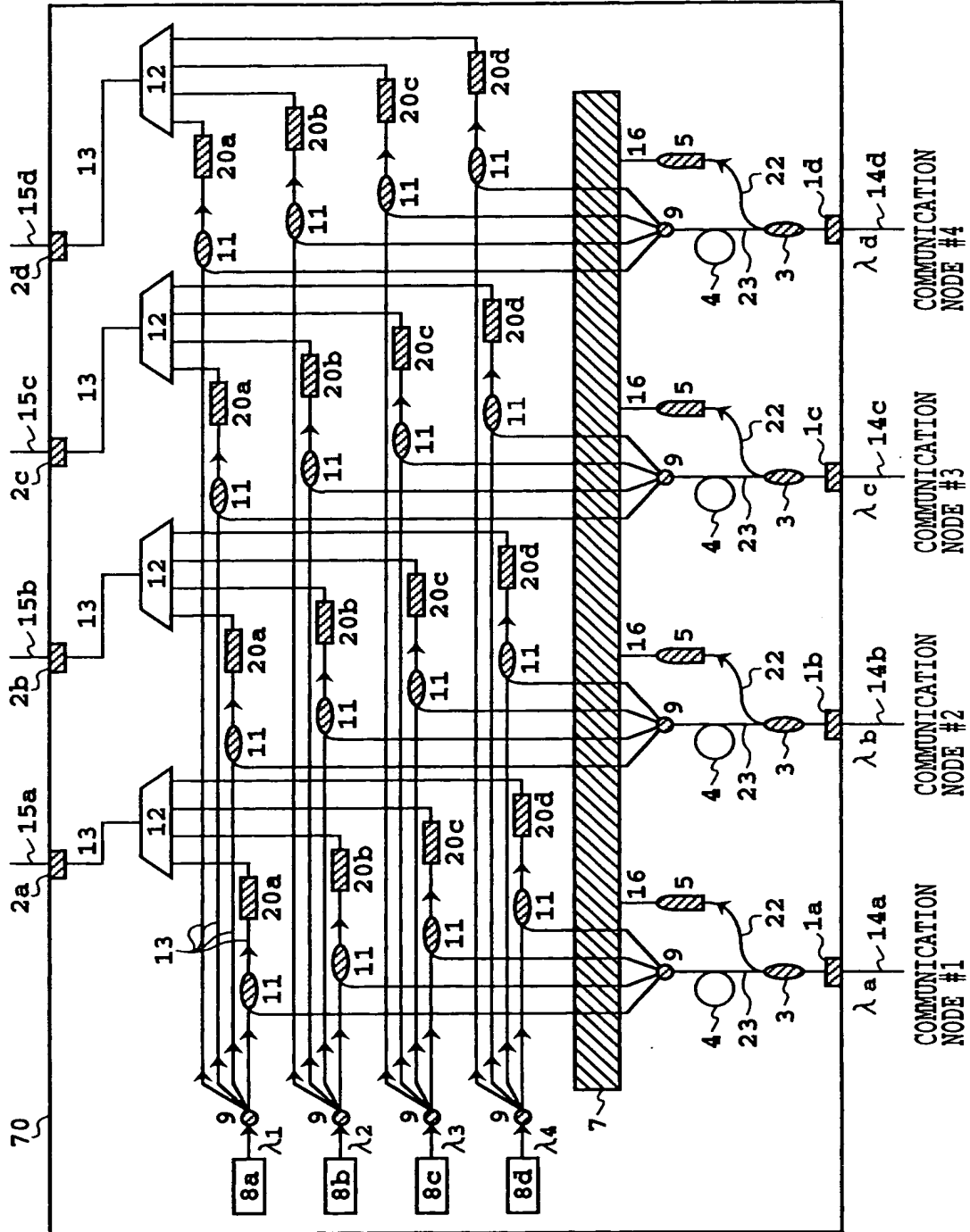
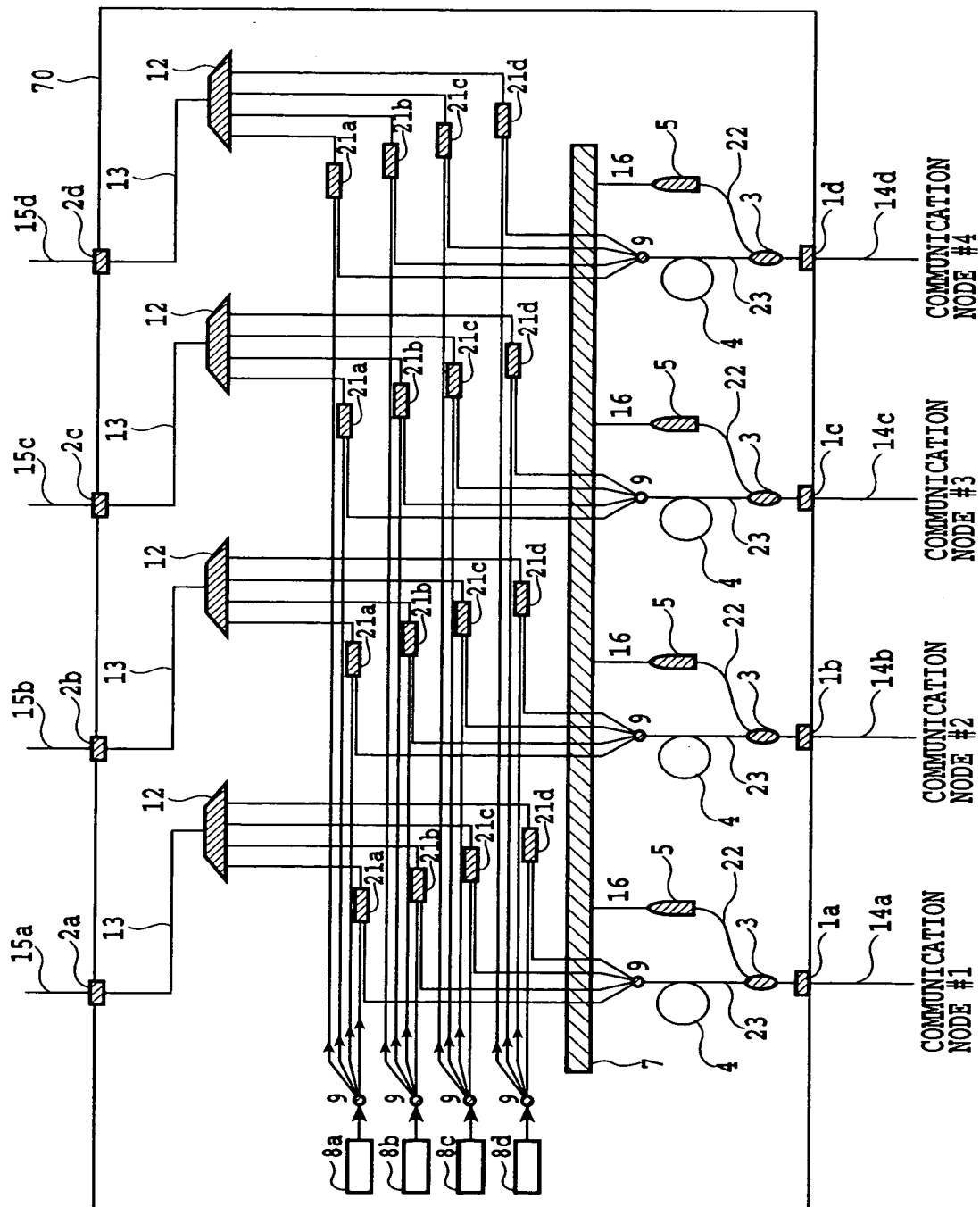


FIG.9

FIG. 10



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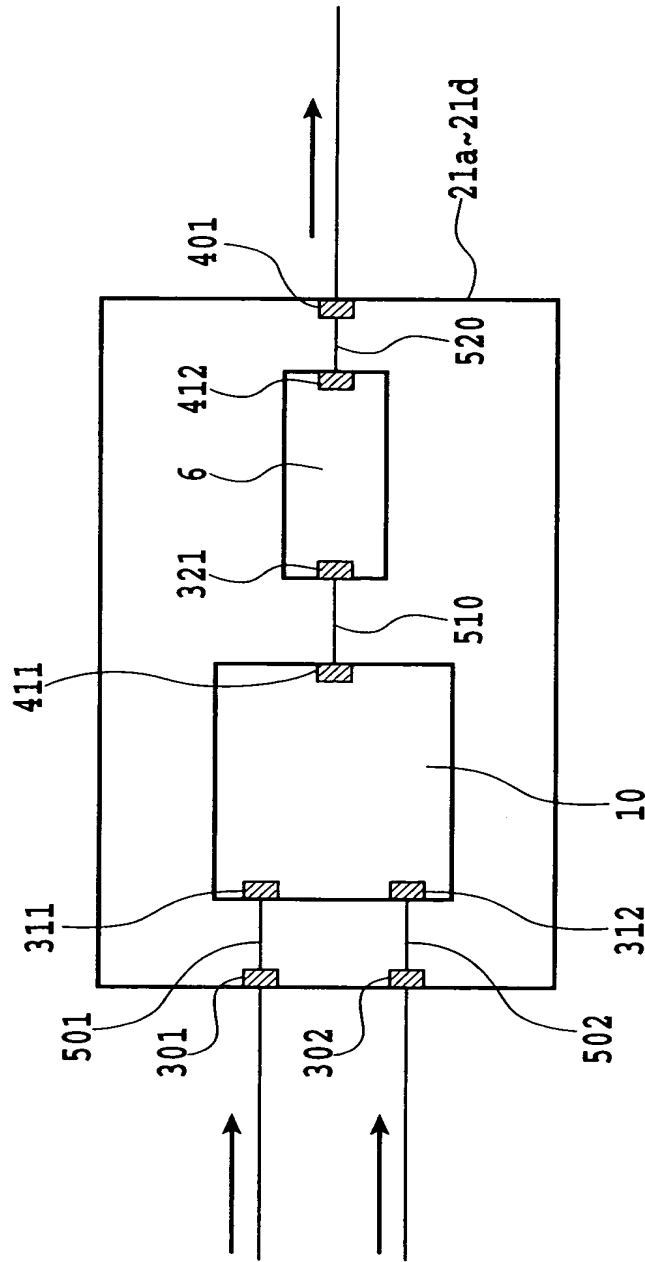


FIG.11

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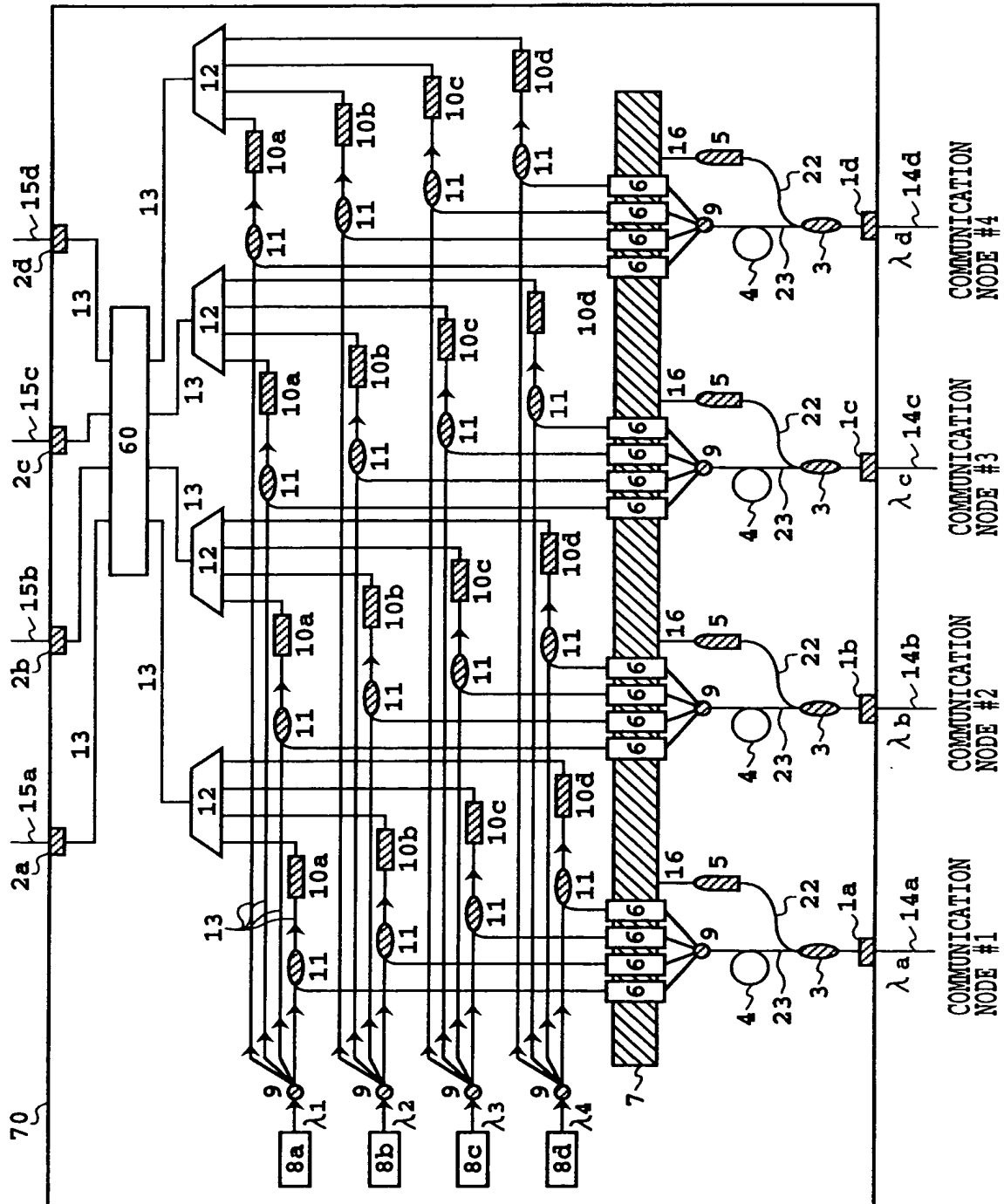


FIG.12

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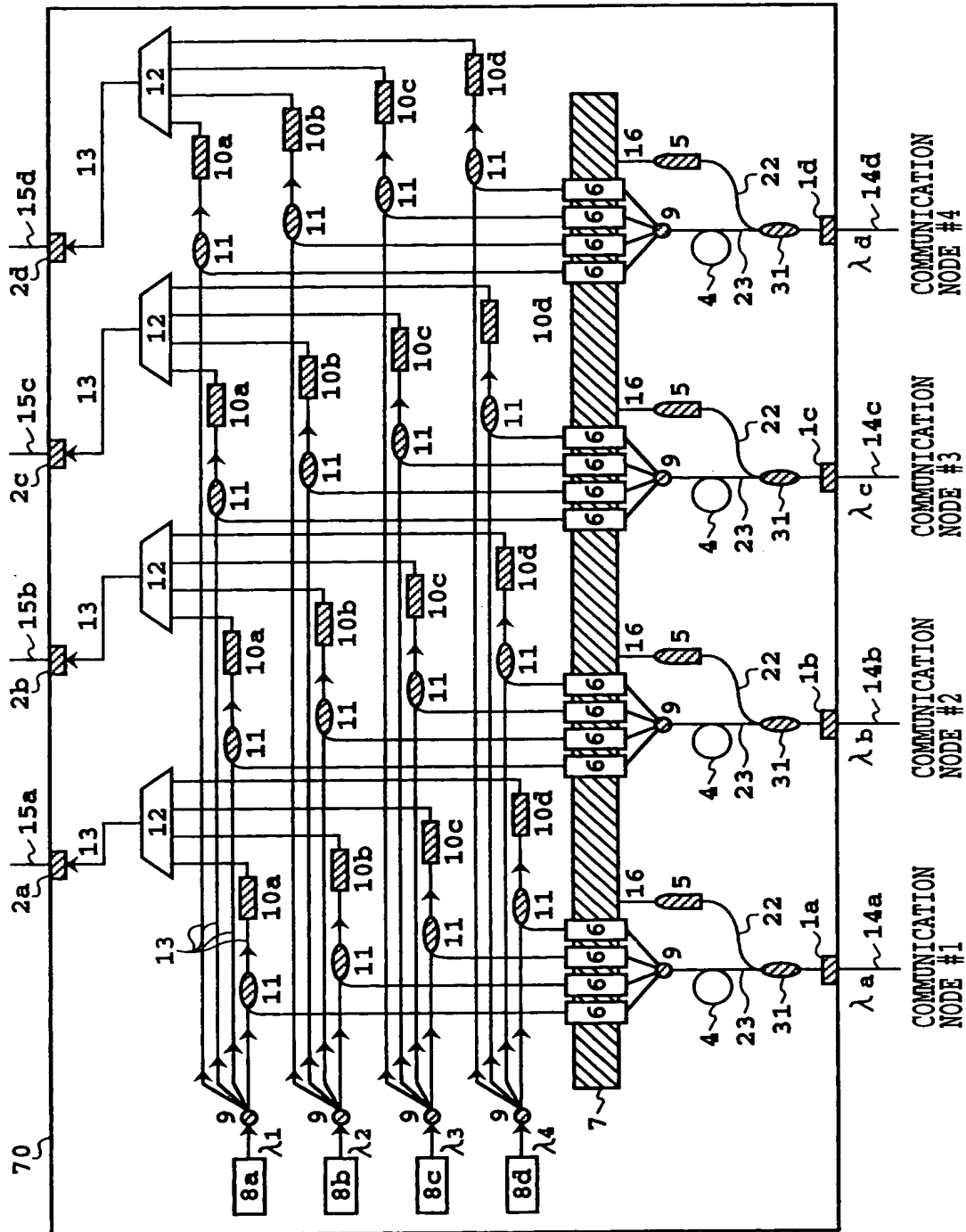
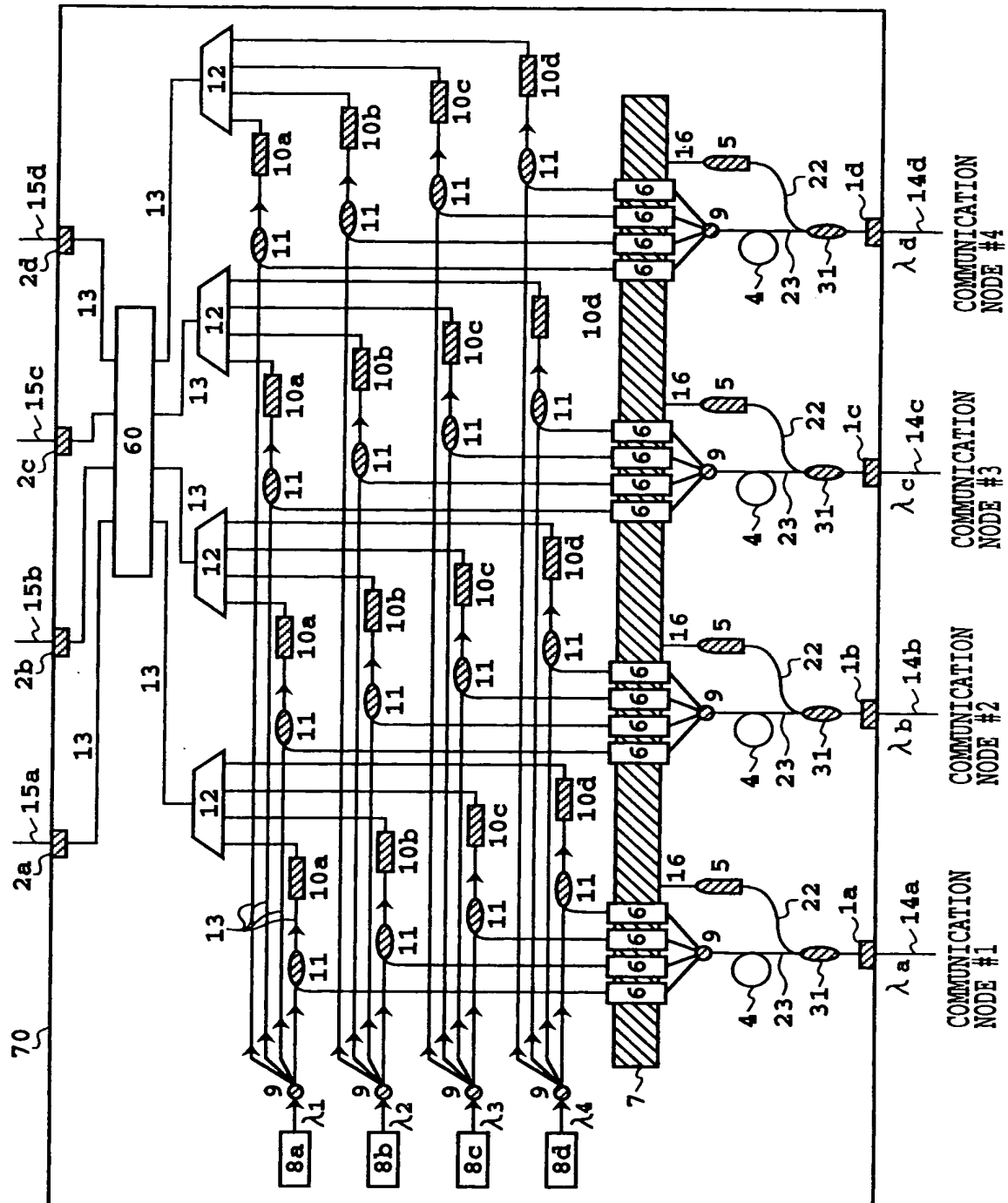


FIG.13



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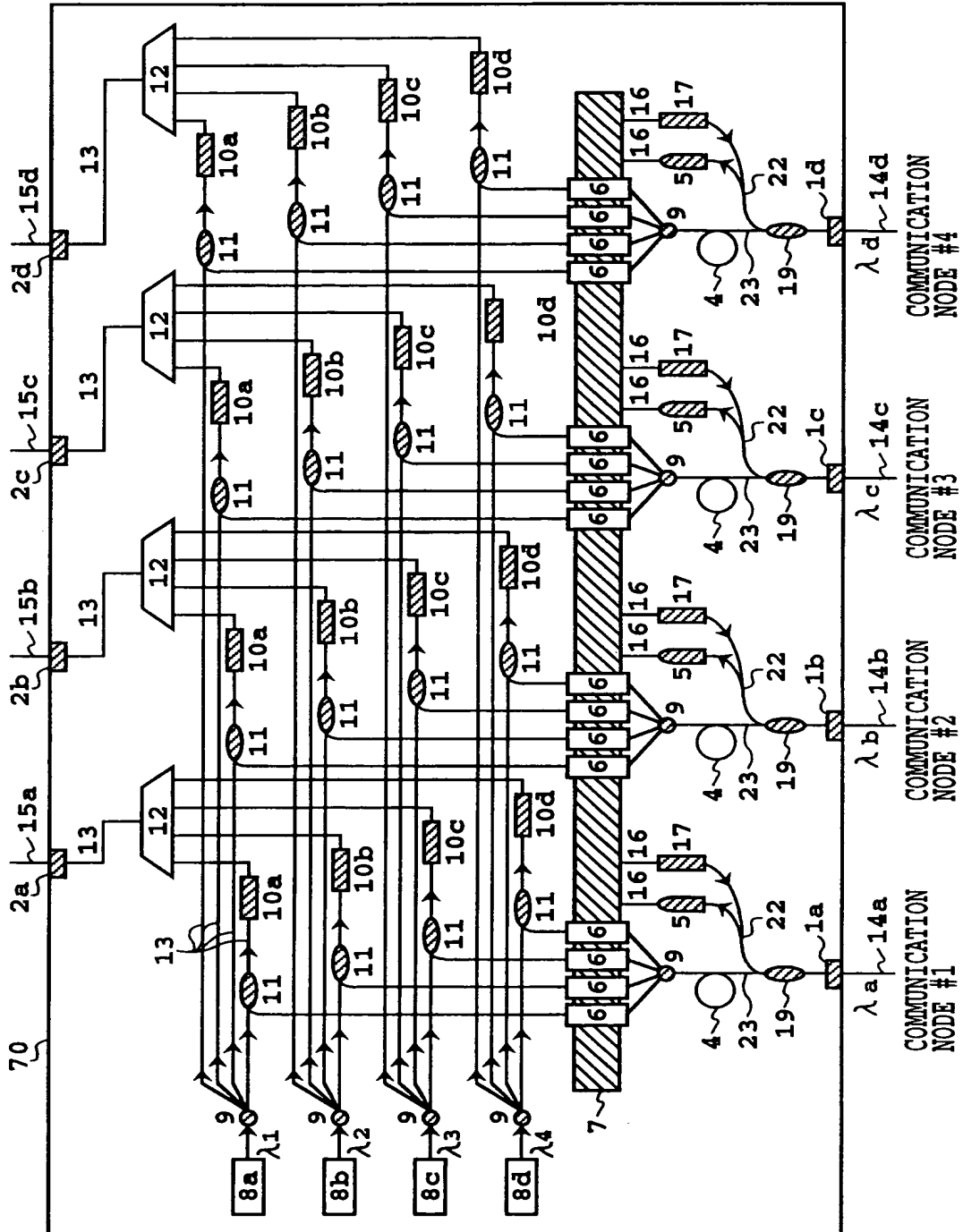


FIG.15

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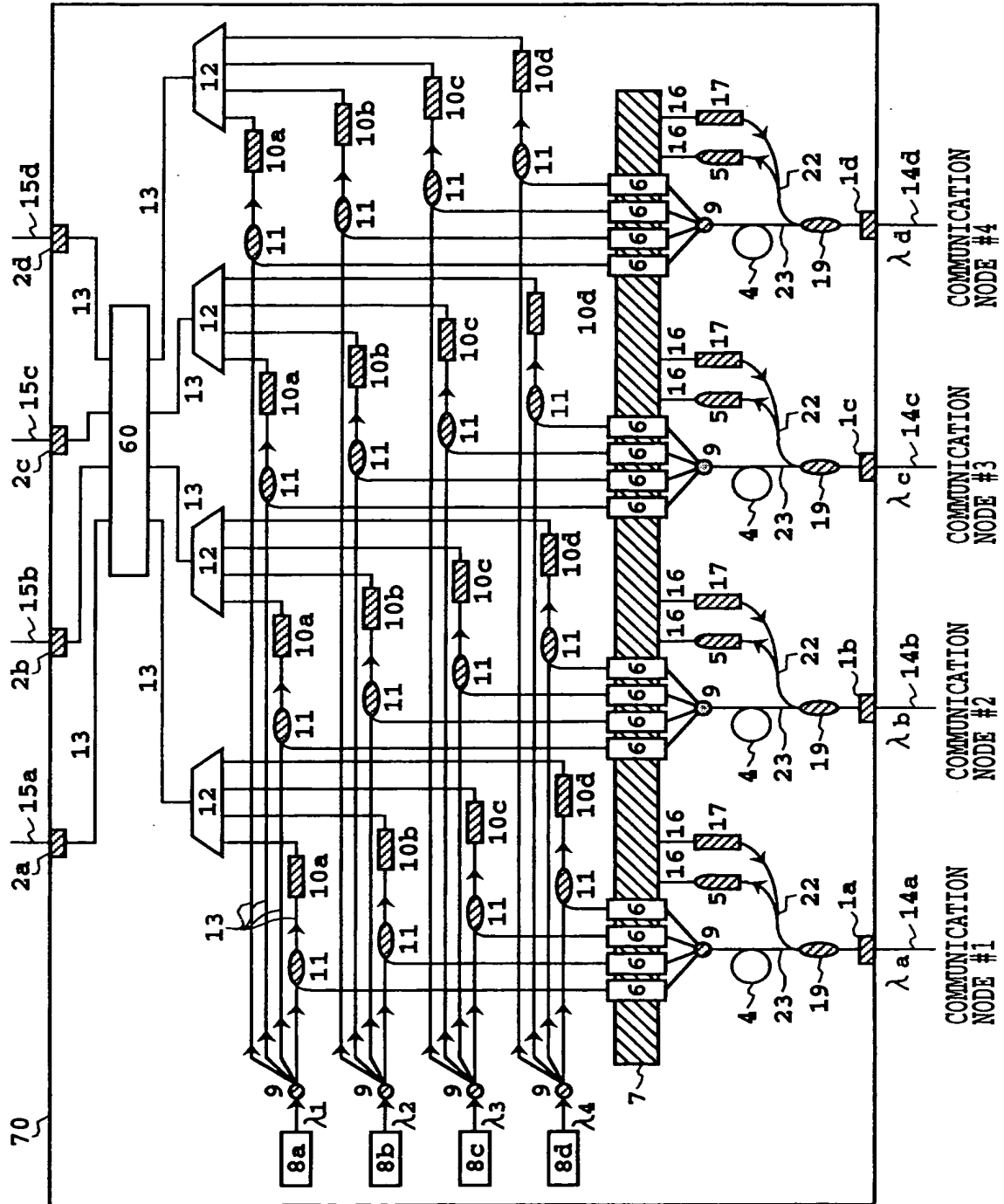


FIG.16

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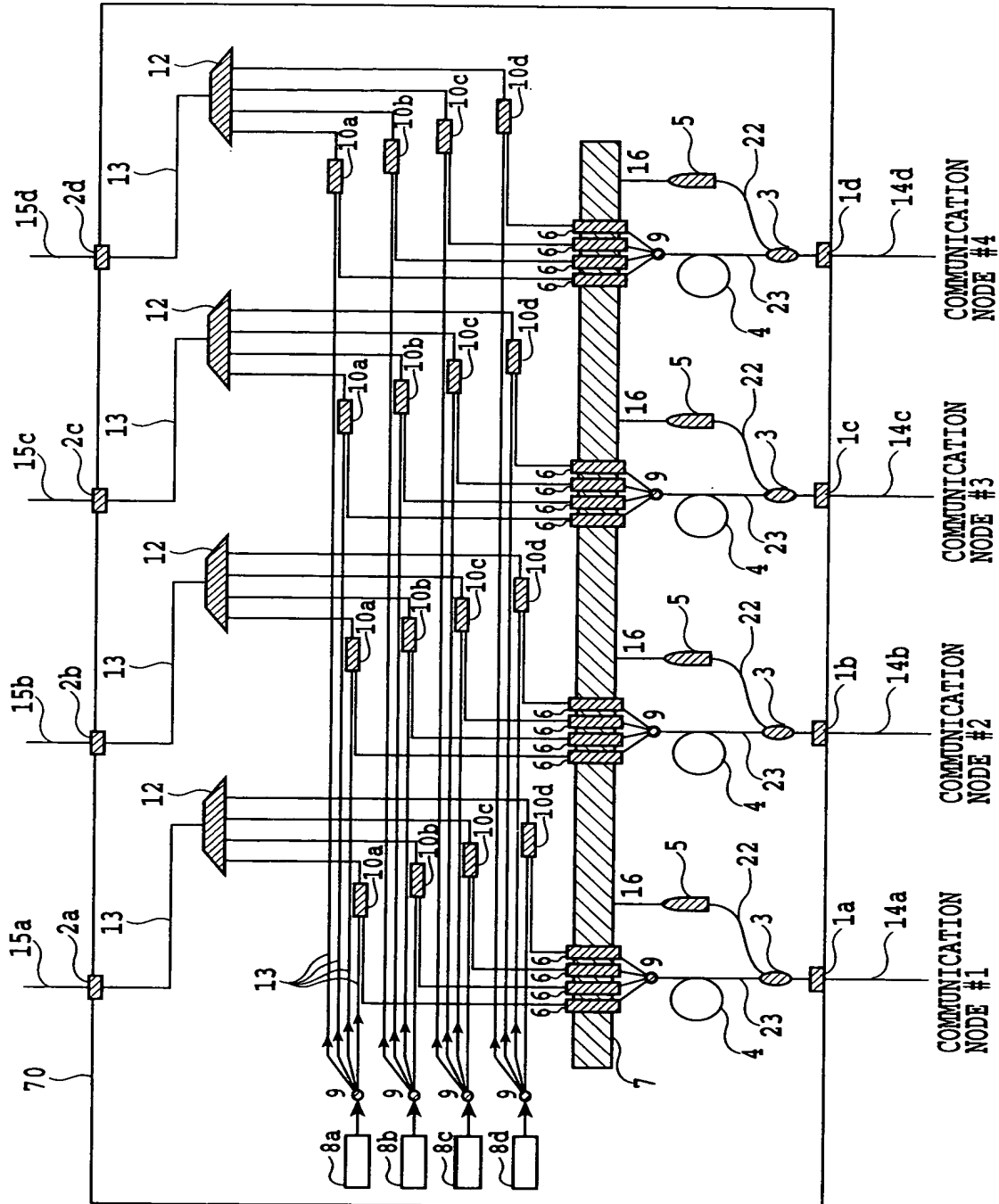


FIG.17

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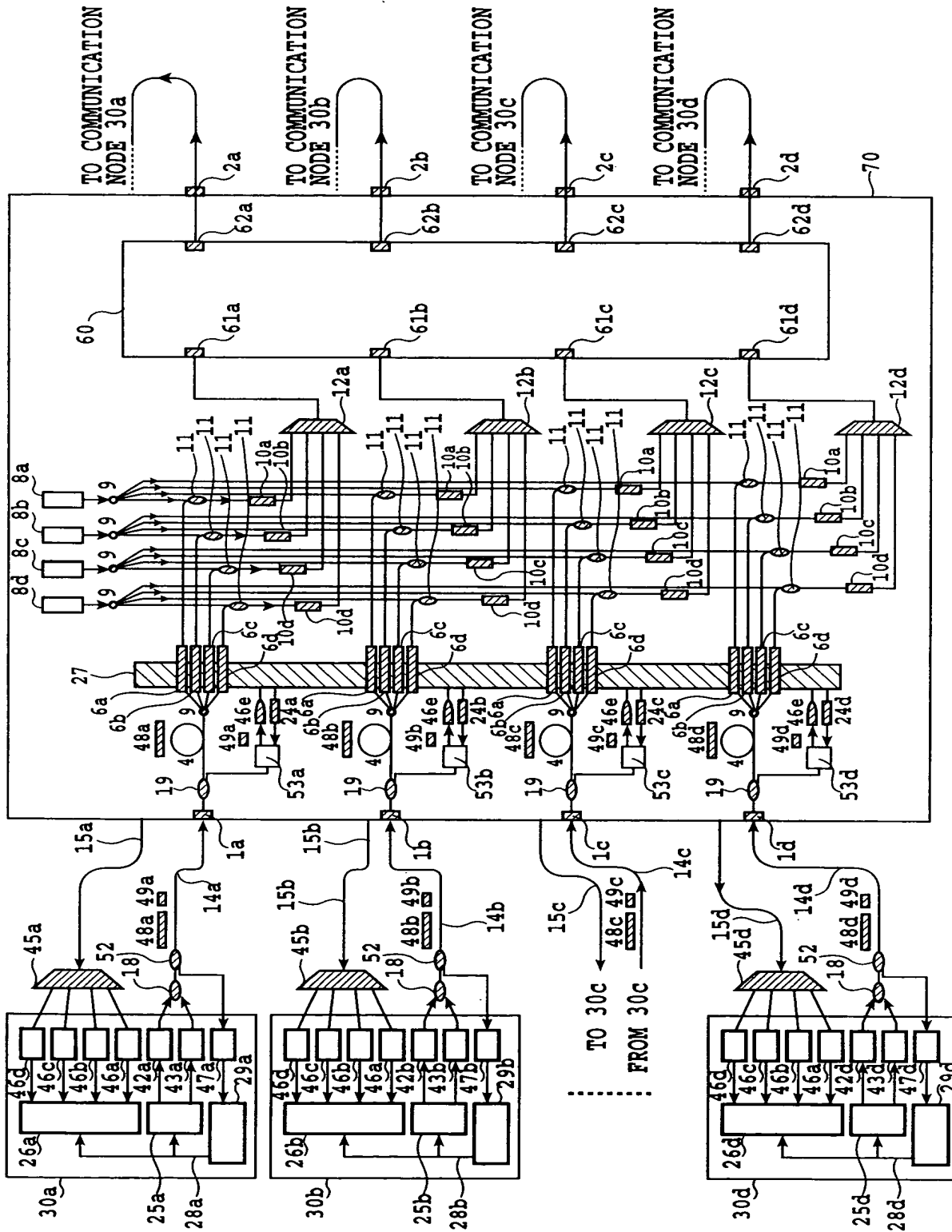
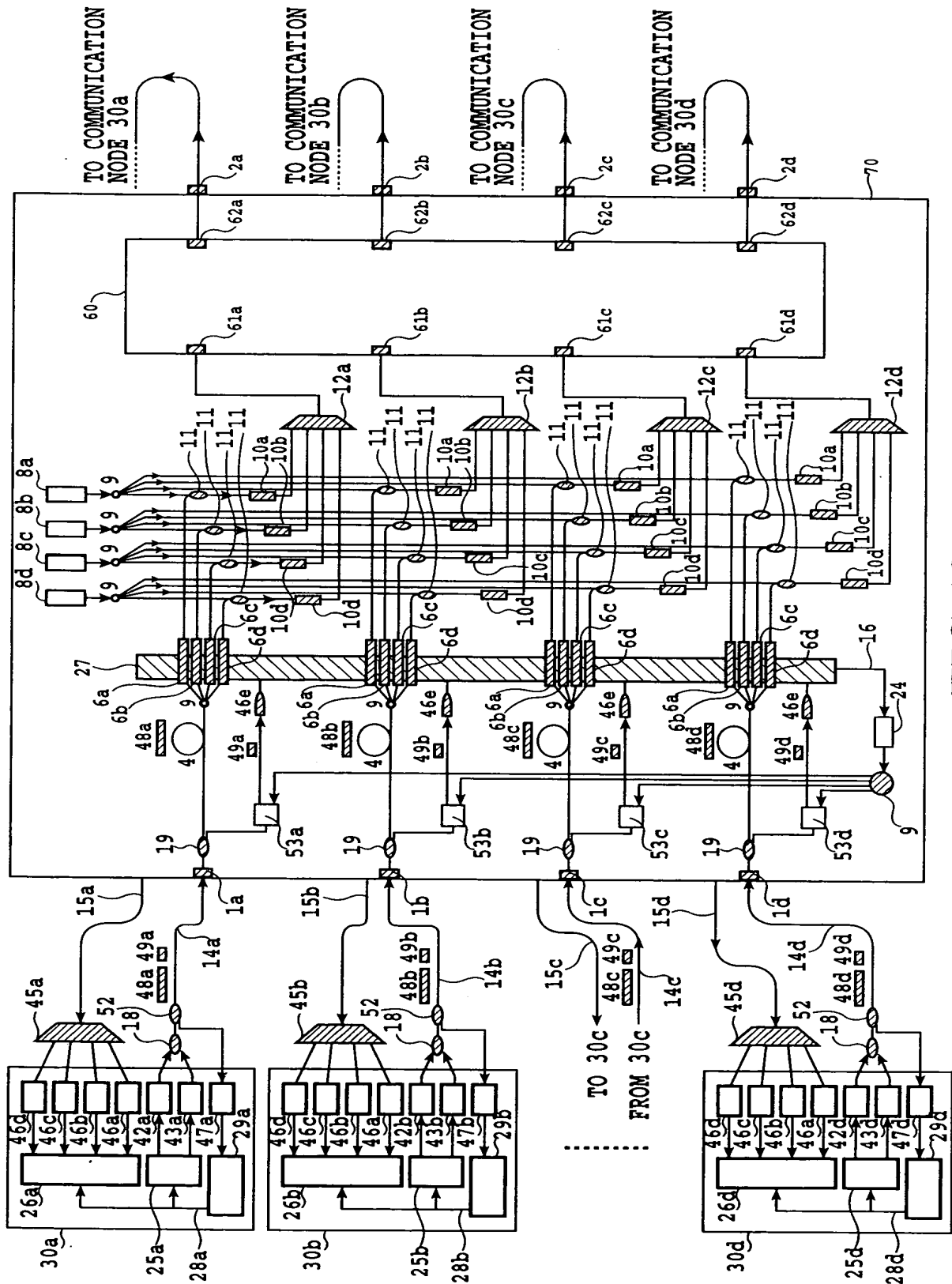


FIG.18



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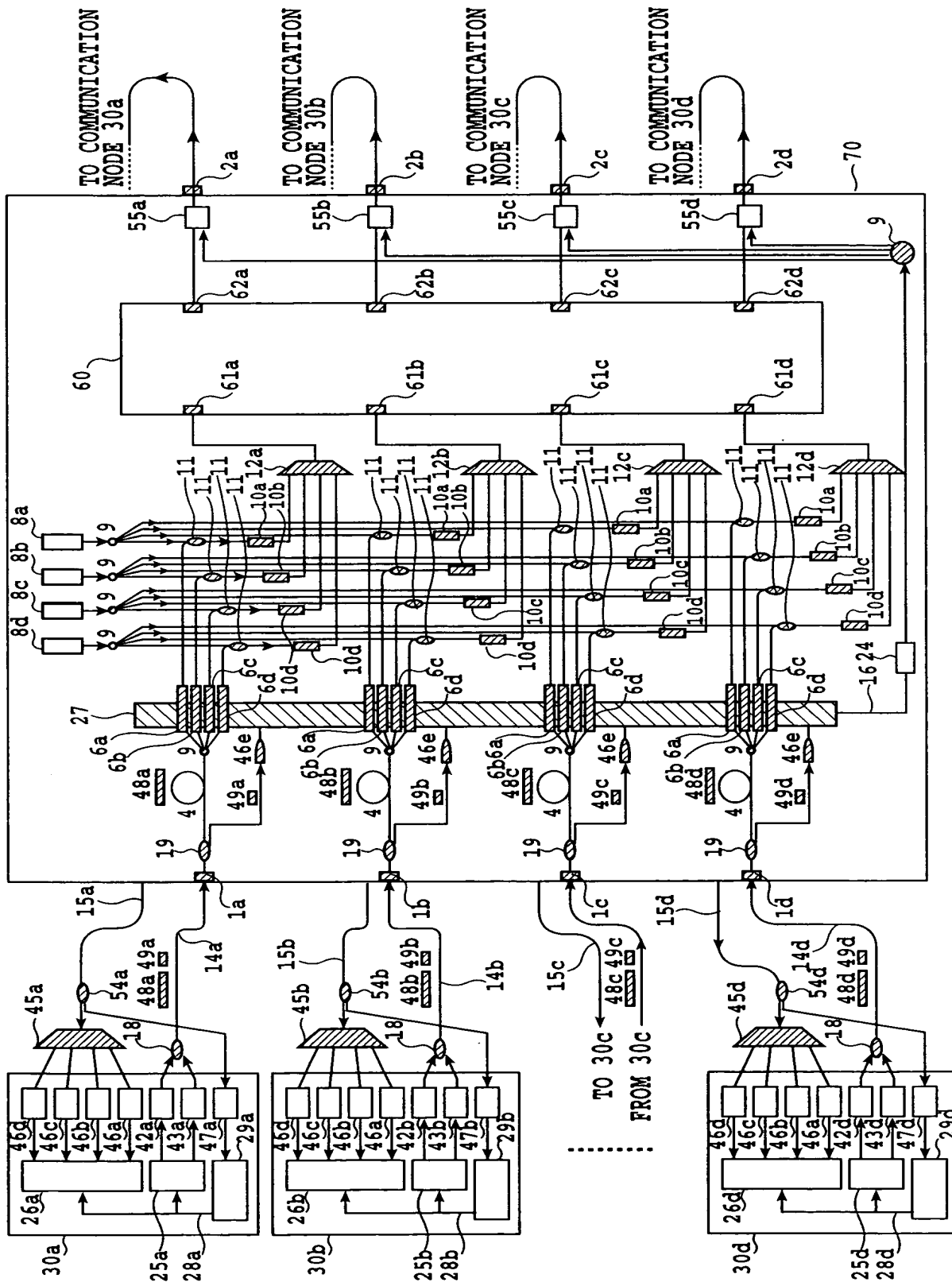


FIG. 20

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		OUTPUT PORT			
		62a	62b	62c	62d
INPUT PORT	61a	λ_a	λ_b	λ_c	λ_d
	61b	λ_b	λ_c	λ_d	λ_a
	61c	λ_c	λ_d	λ_a	λ_b
	61d	λ_d	λ_a	λ_b	λ_c

FIG.21

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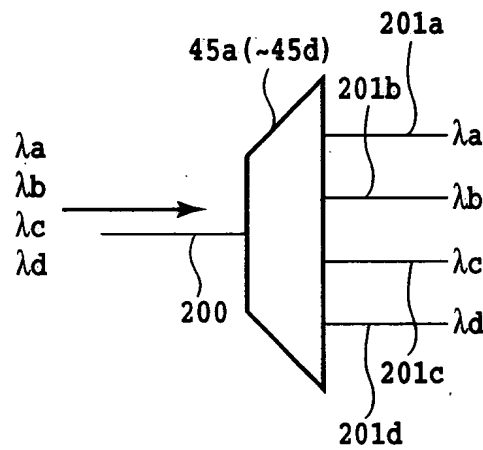


FIG.22

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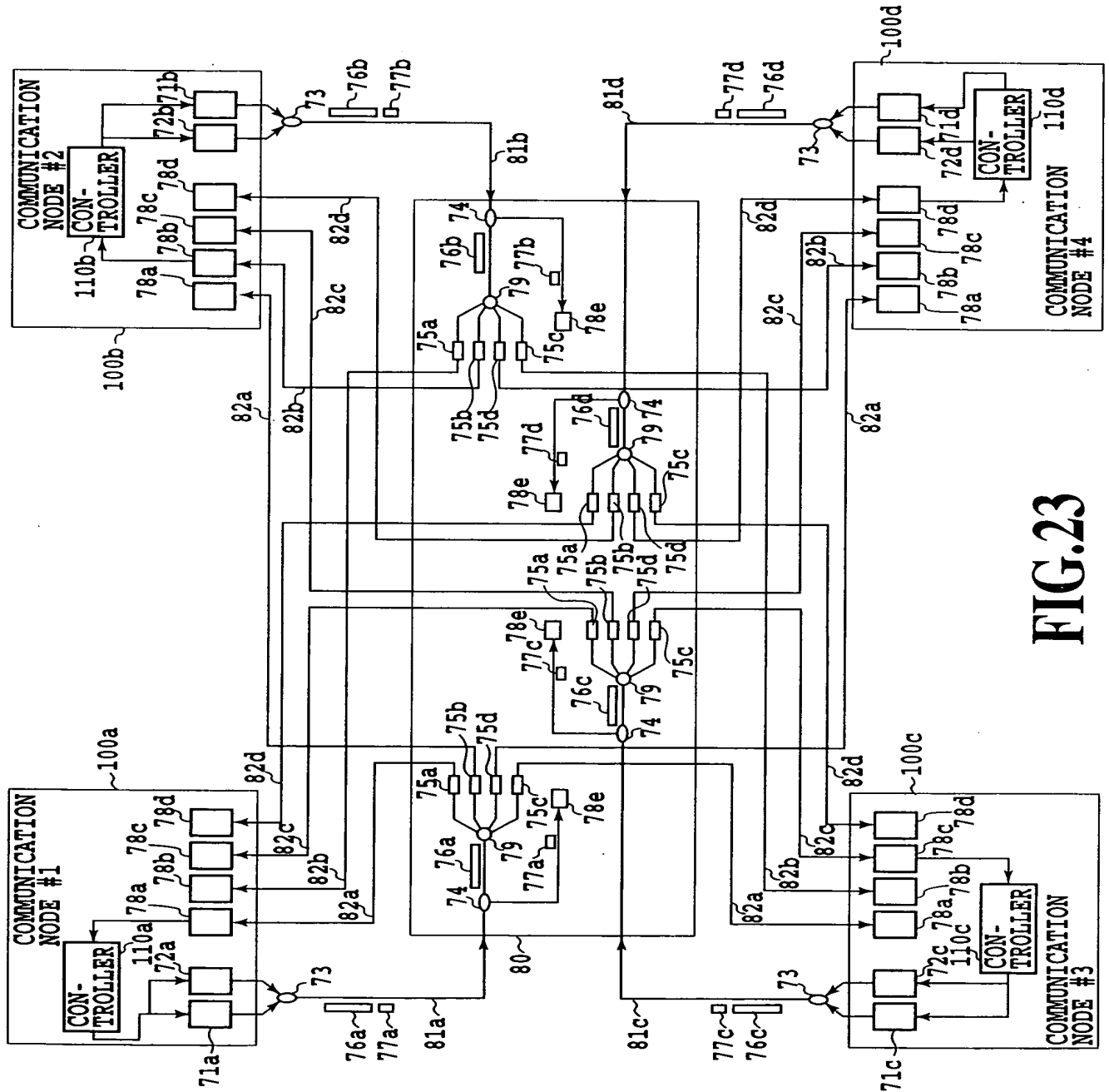


FIG. 23

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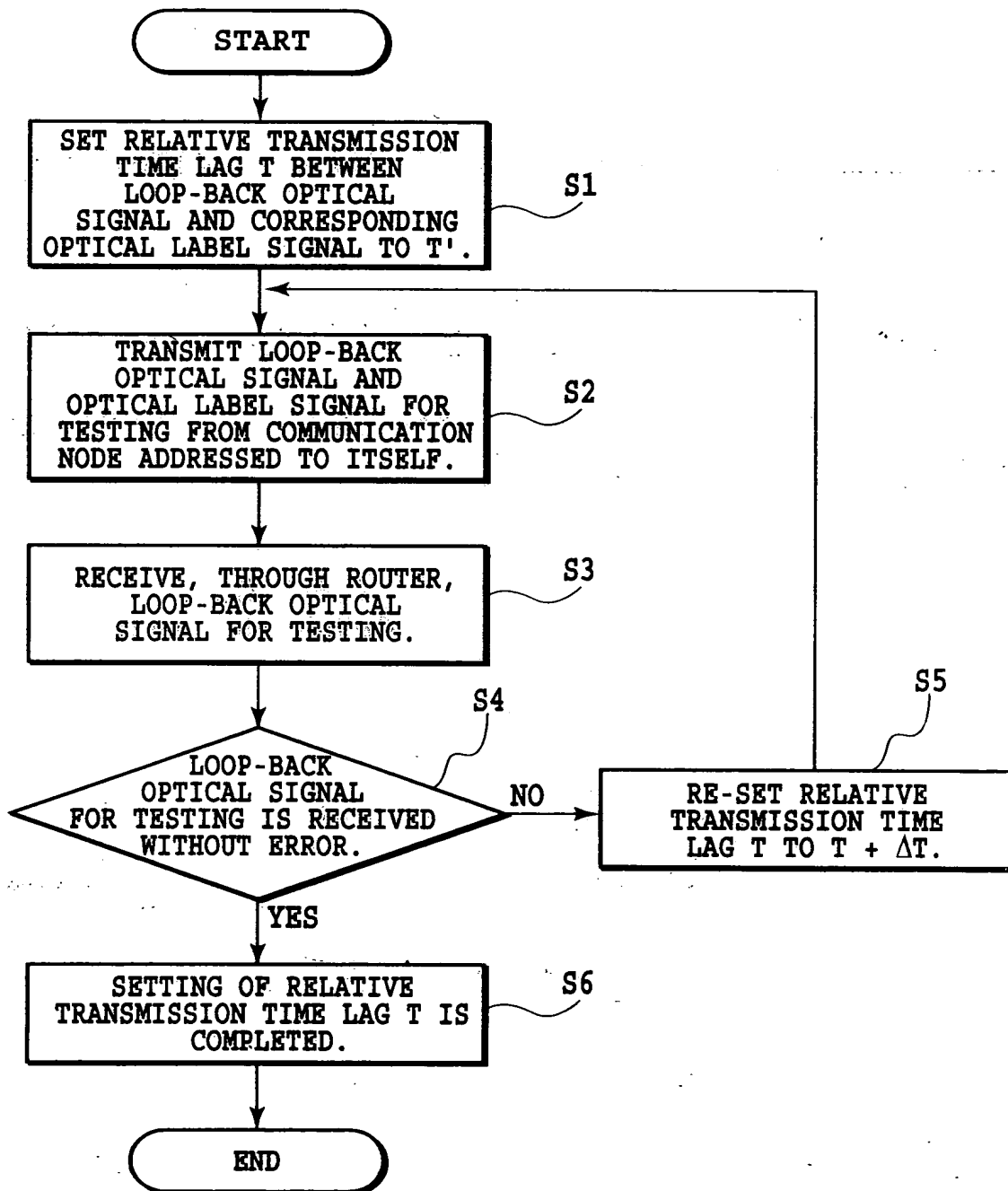


FIG.24

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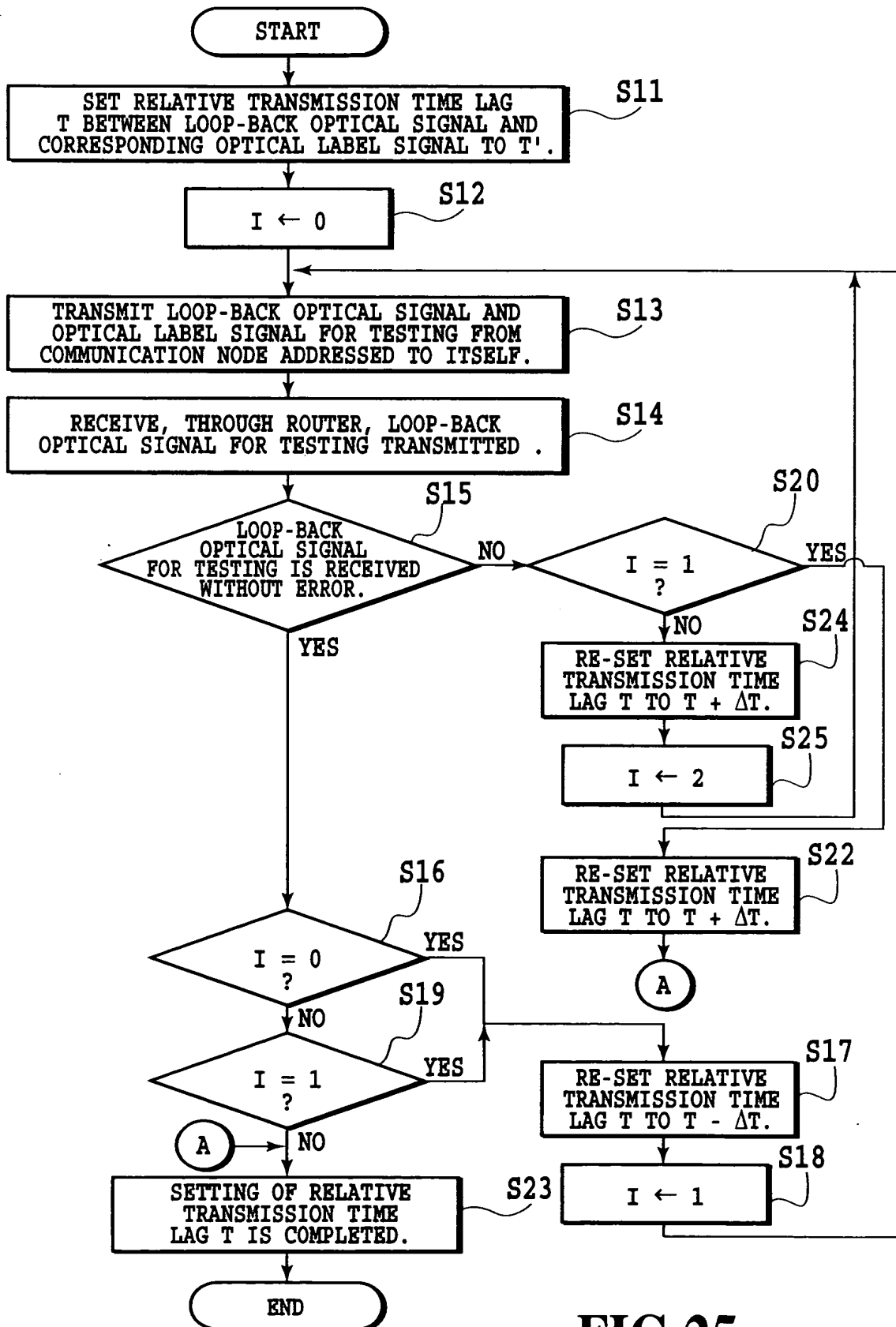


FIG.25

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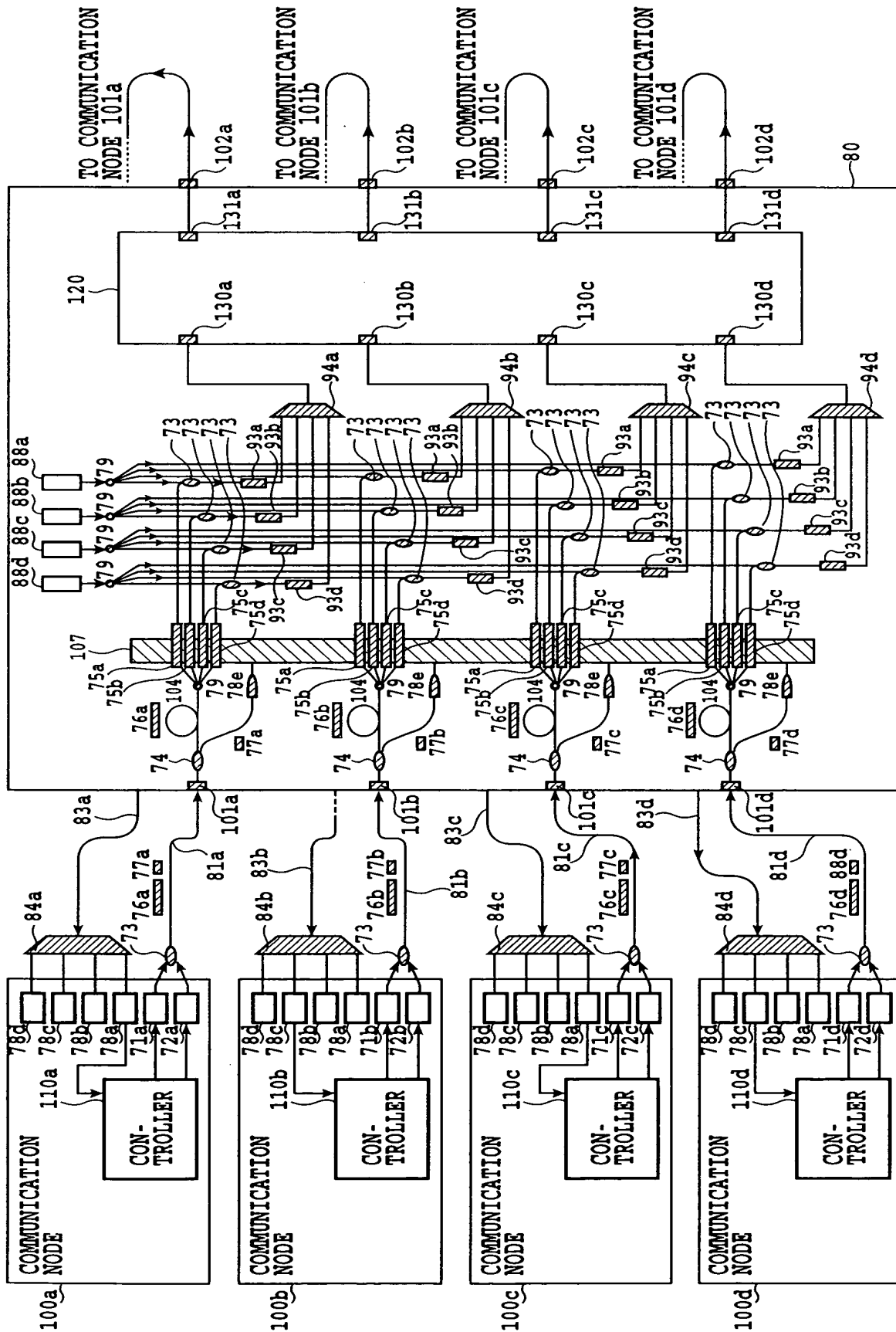


FIG. 26

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		OUTPUT PORT			
		131a	131b	131c	131d
INPUT PORT	130a	λ_a	λ_b	λ_c	λ_d
	130b	λ_b	λ_c	λ_d	λ_a
	130c	λ_c	λ_d	λ_a	λ_b
	130d	λ_d	λ_a	λ_b	λ_c

FIG.27

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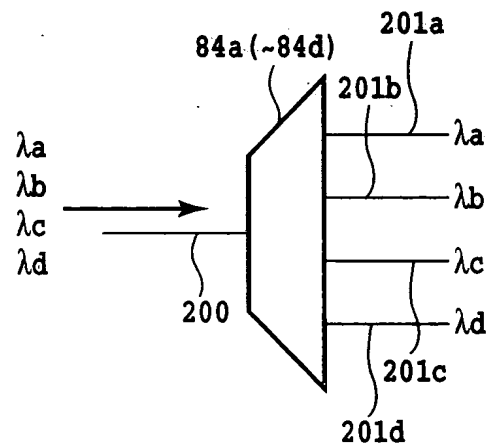


FIG.28